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MS-7B19

mATX
Ver: 10

Coffeelake Platform

CPU: Coffeelake S

PCH: B360

SPI ROM : 128 MB

Memory: DDR4 * 4 (Dual Channel)

Power Solution:

CPU : RT3607

VCCSA : NB685

VCCIO : SY8288

DDR : RT8231

PCH : RT8125E

ACPI: MPS

Onboard Chip:

LAN RTL8111H

Dual Codec: ALC887

SIO: NTC6797

Type C: ASM1543

USB3 Redrive : ASM1464 X 1

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

M.2 Slot (Socket 1) * 1

LED

EZ Debug LED

Audio Line LED

Rear I/O Connectors

PS2

USB2.0x2

USB3.1 Gen1x4

RJ45 + USB3.1 (Type C+ A)

Audio Jack 3 Port

HDMI+DVI+VGA)

Internal Connectors

Dual SATA * 3

FUSB3.0 Header * 1

FUSB2.0 Header * 2

Front Audio Header * 1

Front Panel Header * 2

SPI Header * 1

TPM Header * 1

CPU Fan * 1

System Fan * 2

Internal Pin Header

JRGB1

JCI1

JCOM1

JSPI1

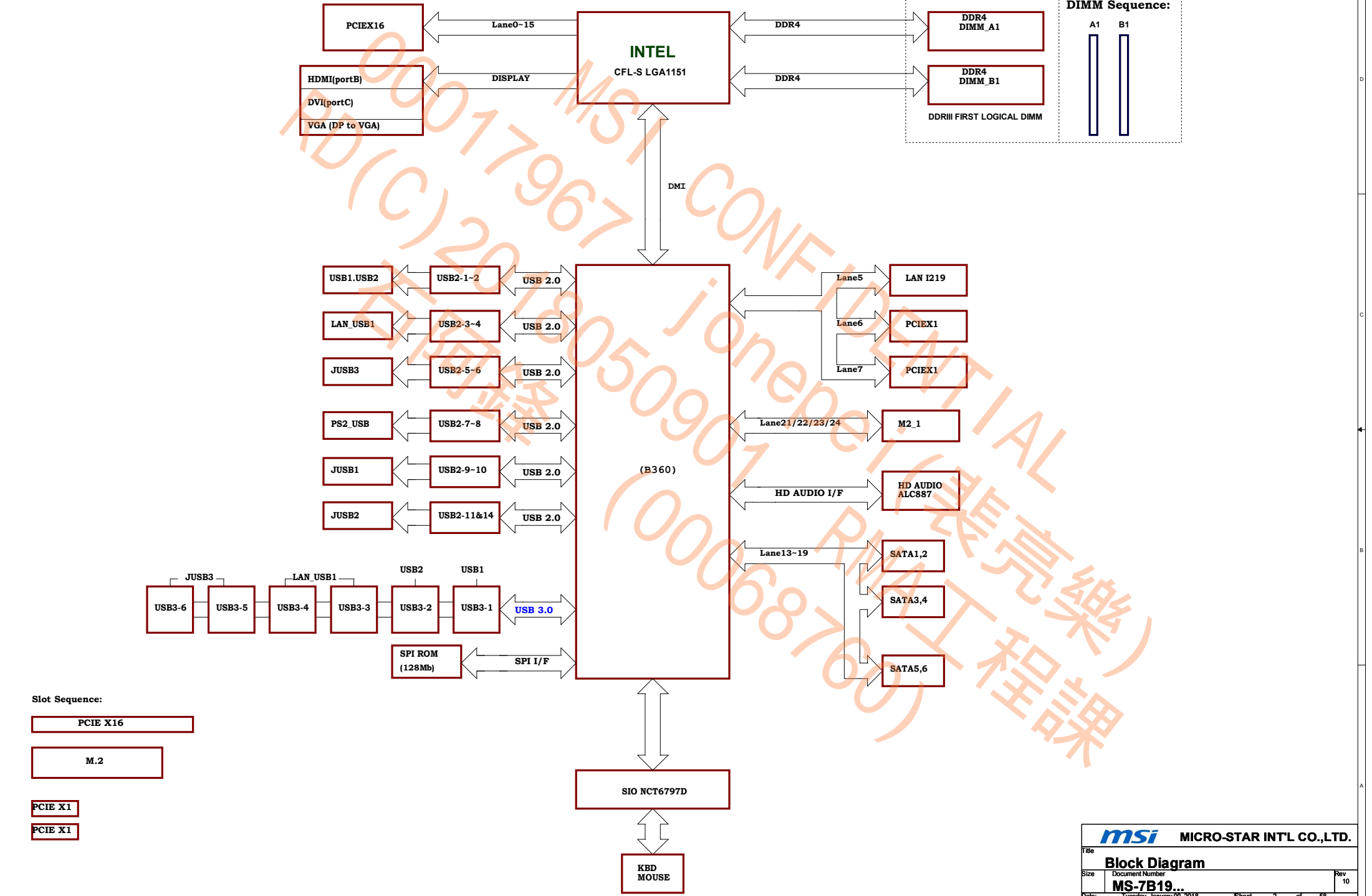
JBAT1

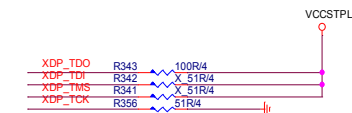
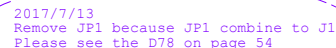
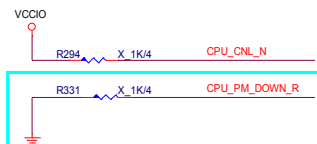
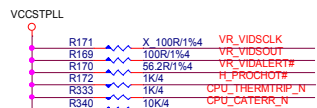
JTPM1

JLPT1

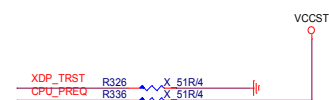
msi MICRO-STAR INT'L CO.,LTD.		
Title Cover Sheet		
Size	Document Number	Rev
	MS-7B19...	10
Date:	Tuesday, January 09, 2018	Sheet 1 of 58

MS-7B19 Block Diagram



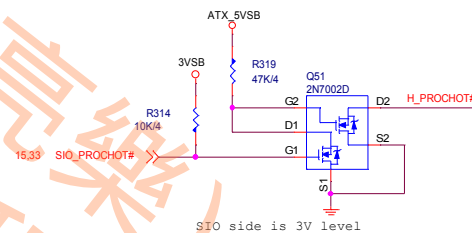
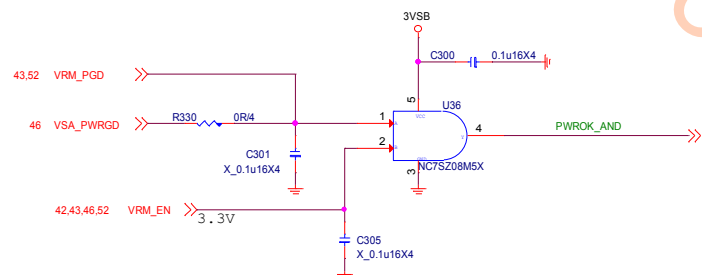


Close CPU <1100 mil
1000 mil < CPU XDP MBP0~1 < 6000 mil



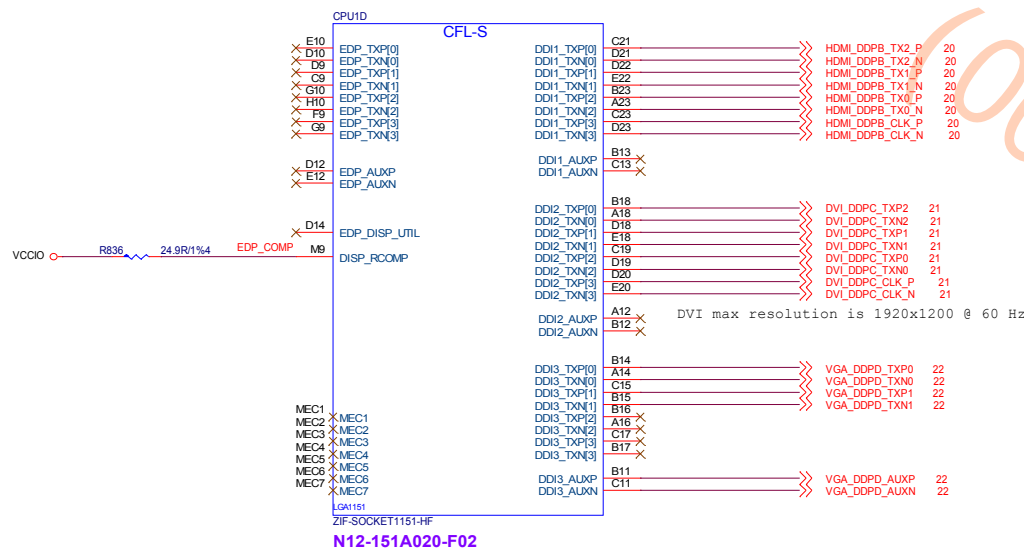
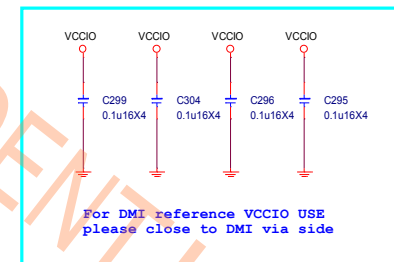
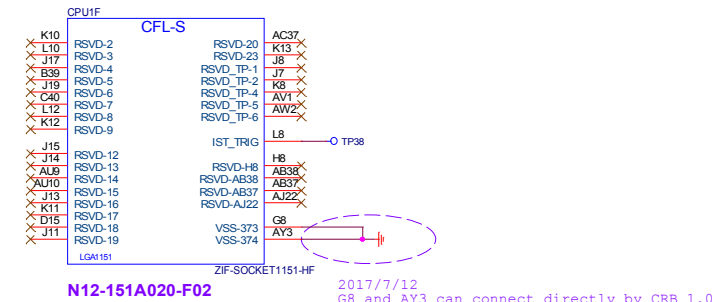
11/30 Modify for SILEGO Sequence

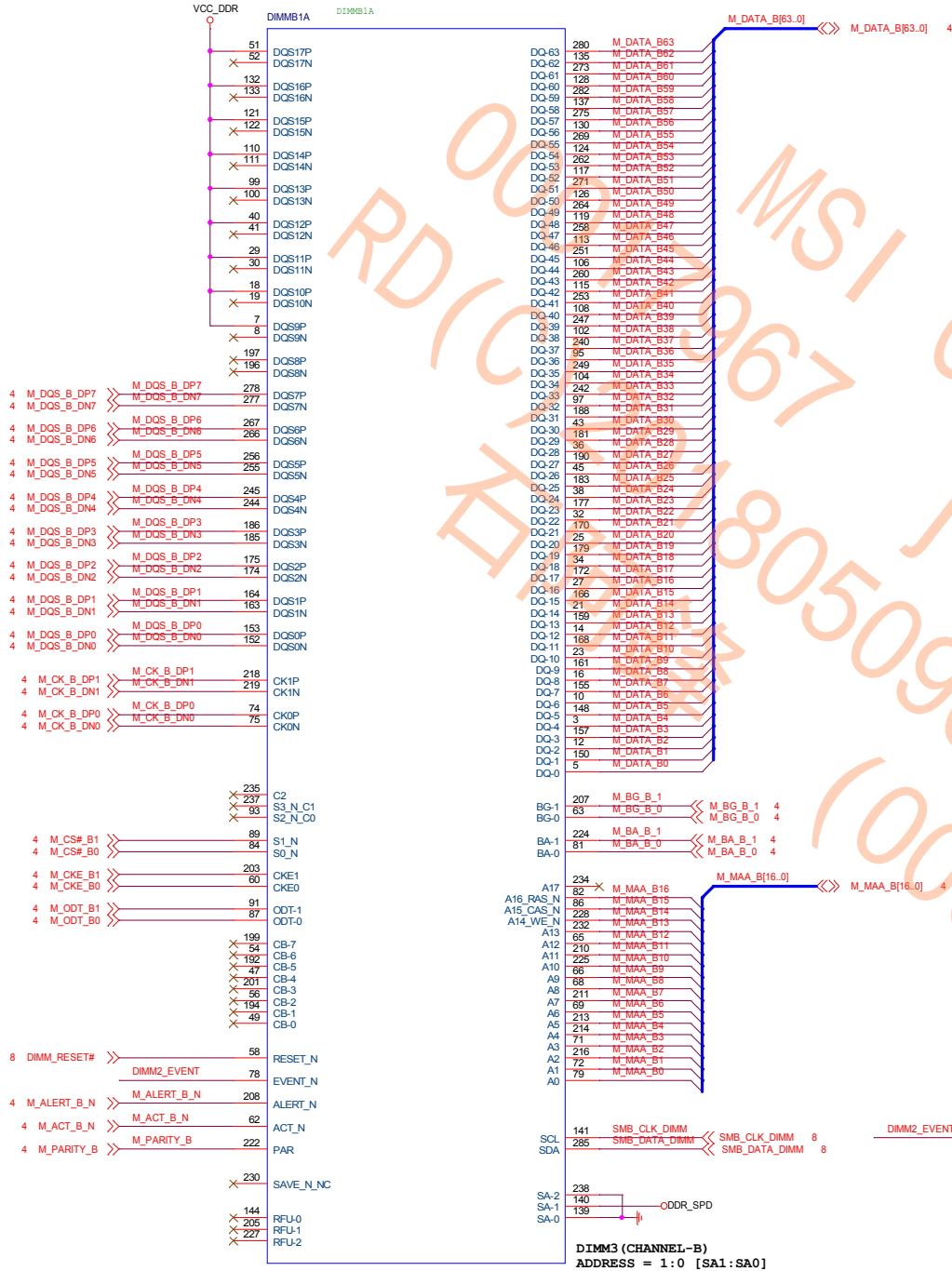
MP Remove?



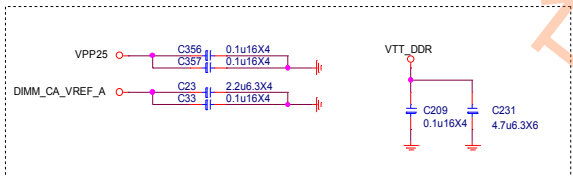
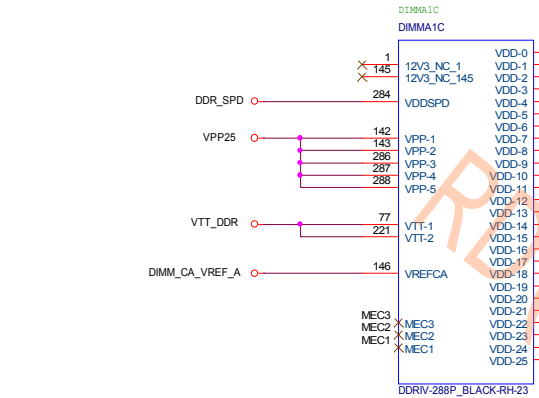
CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	GDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG CFEER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

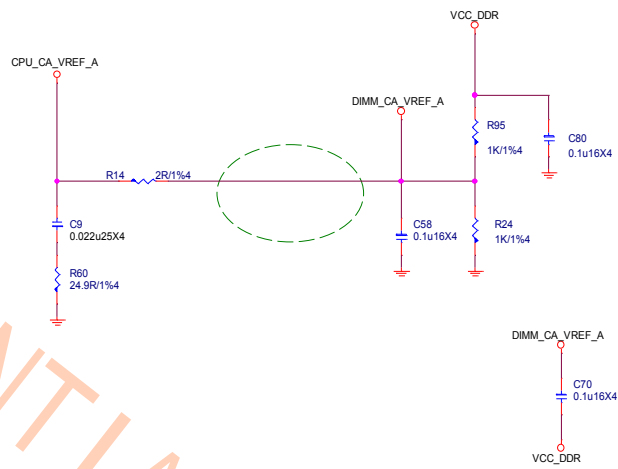
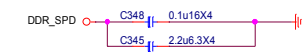
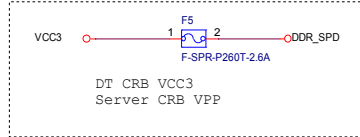
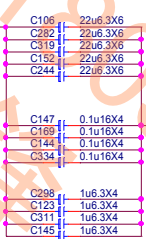
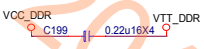
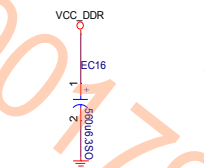


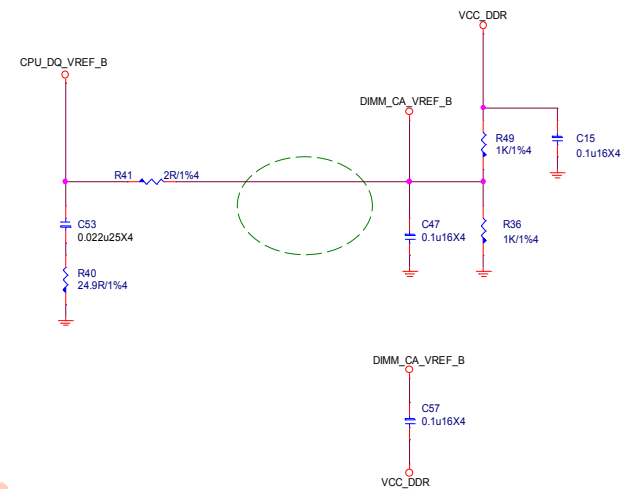
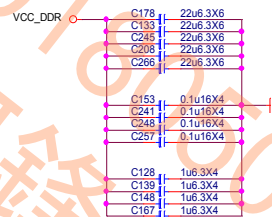
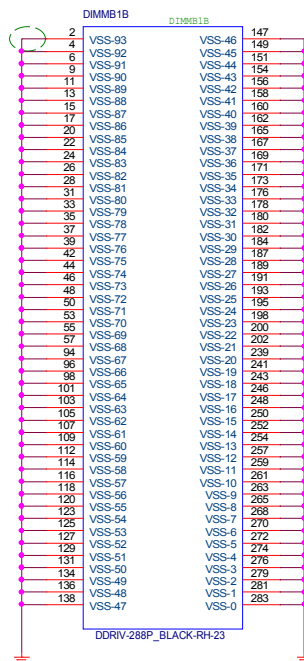
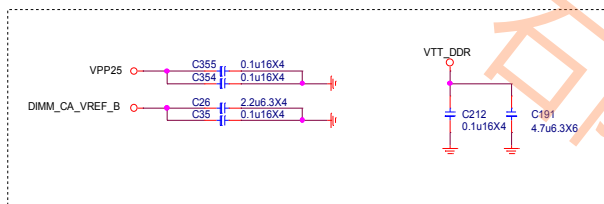
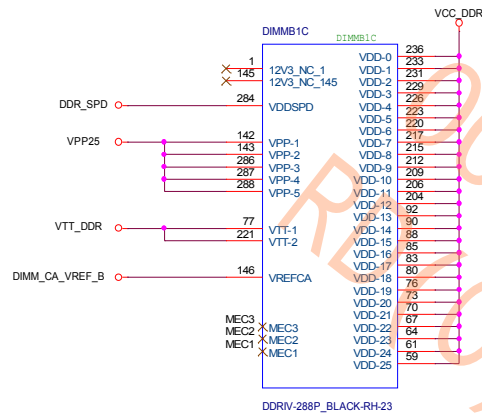


DDR4-288P_BLACK-RH-23
N13-2880681-L06



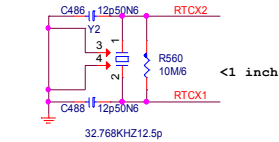
DIMM SLOT PN BY SPEC



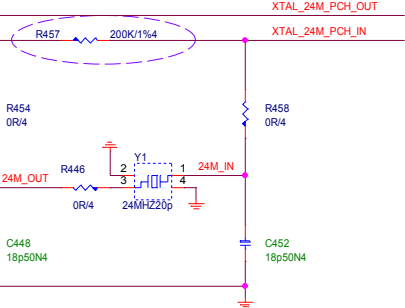


PCH_CLK

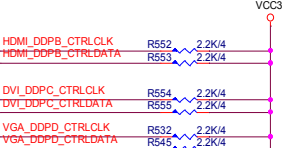
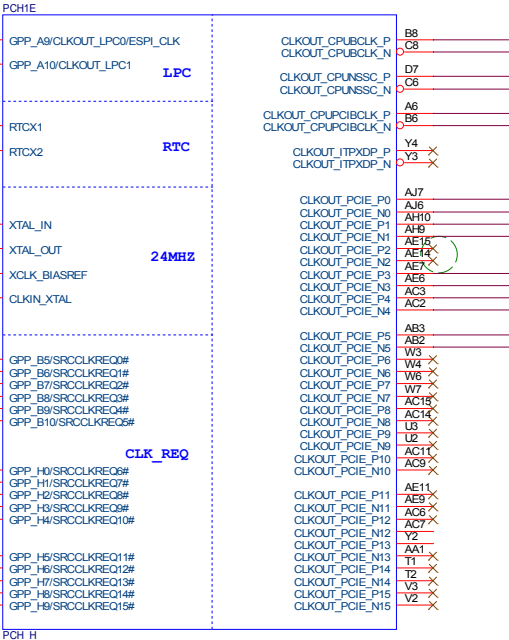
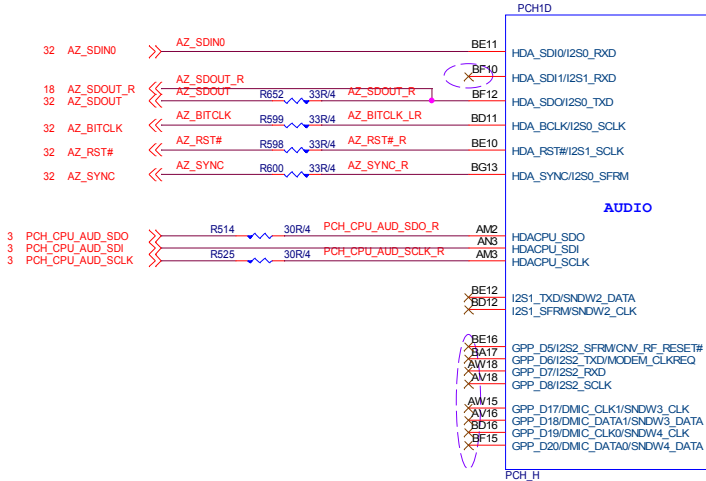
Close to PCH



2017/7/11
The value of R689 is the same as PDG r0.9 by Intel's feedback



PCH_AUDIO

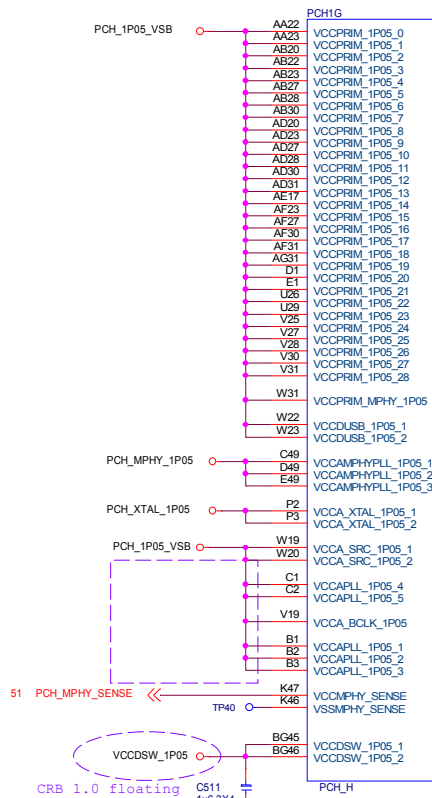
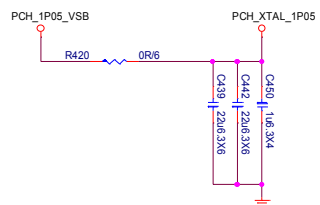
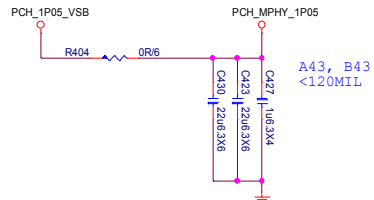


Internal pull-down is disabled after PCH_PWROK is high.

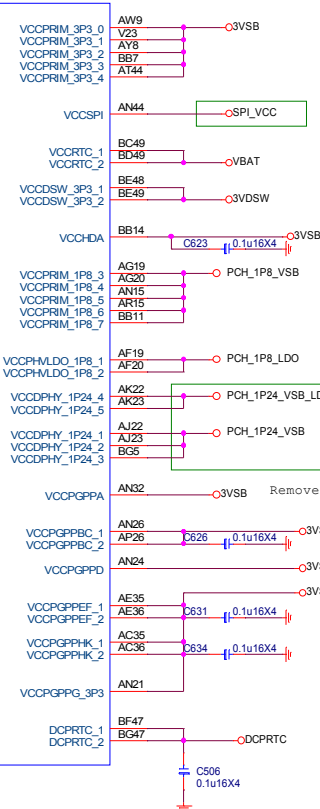
0 : Port B is not detected.(Default)
1 : Port B is detected.

0 : Port C is not detected.(Default)
1 : Port C is detected.

0 : Port D is not detected.(Default)
1 : Port D is detected.

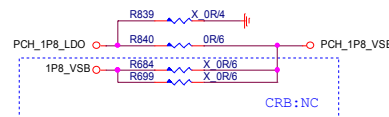


POWER



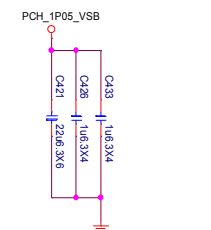
171213 Change to SPI_VCC

PCH_1P24_VSB R1028 X 0R6 PCH_1P24_VSB_LDO
171212 Modify for Intel update
with CNVI R1028 stuff
no CNVI R1028 no stuff

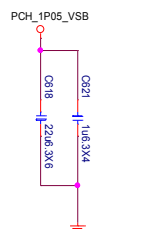


Remove GPPD Colay 1.8V

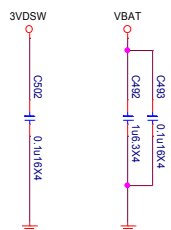
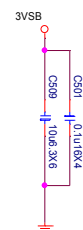
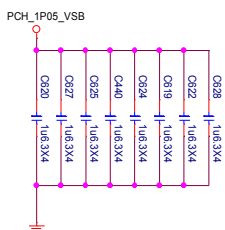
Remove GPPD Colay 1.8V



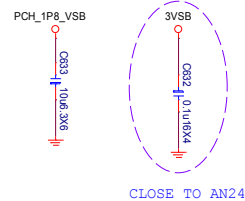
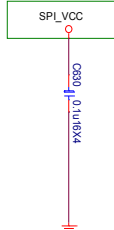
CLOSE TO B1/B2/B3/C1/C2



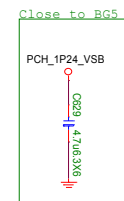
CLOSE TO U26/U29



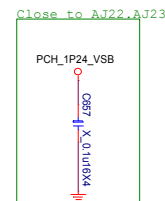
171213 Change to SPI_VCC



CLOSE TO AN24

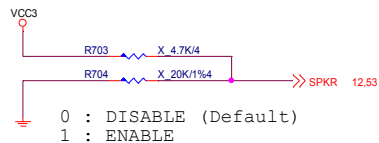


171213 Modify to 4.7uF(PDG)



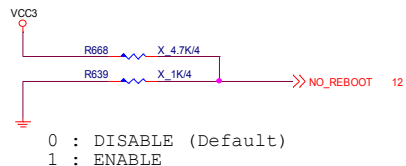
171213 Reserve for AJ22, AJ23

TOP Swap



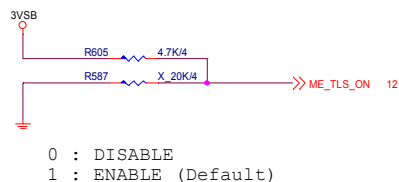
Internal pull-down is disabled after PCH_PWROK is high.

No Reboot



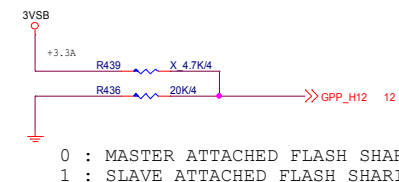
Internal pull-down is disabled after PCH_PWROK is high.

TLS confidentiality



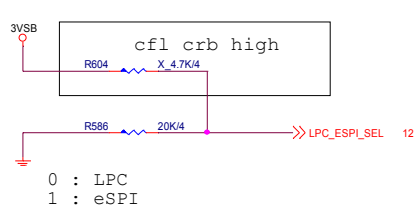
Internal pull-down is disabled after RSMRST# de-assert.

ESPI FLASH SHARING MODE



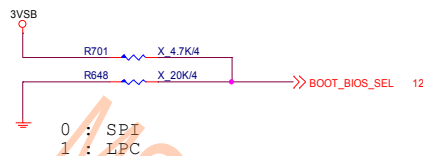
Internal pull-down is disabled after RSMRST# de-assert.

LPC eSPI Mode



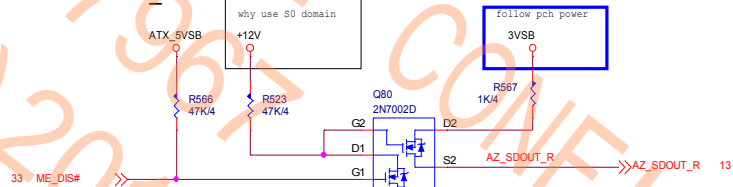
Internal pull-down is disabled after RSMRST# de-assert.

Boot BIOS



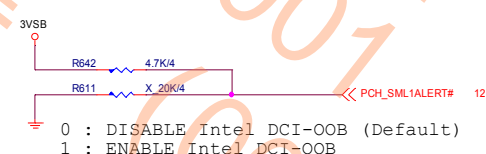
Internal pull-down is disabled after PCH_PWROK is high.

HDA_SDO



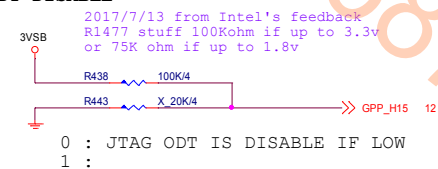
Internal pull-down is disabled after PCH_PWROK is high.

DCI ENABLE



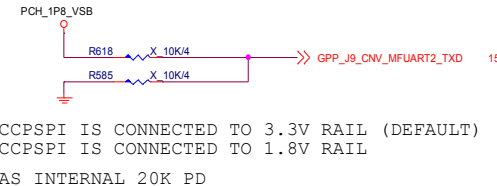
Internal pull-down is disabled after RSMRST# de-assert.

ODT DISABLE



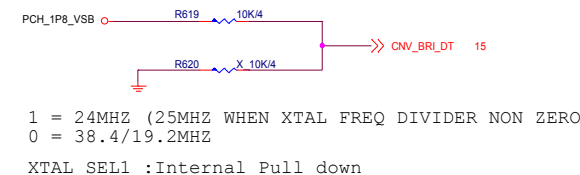
Internal pull-down is disabled after RSMRST# de-assert.

SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE

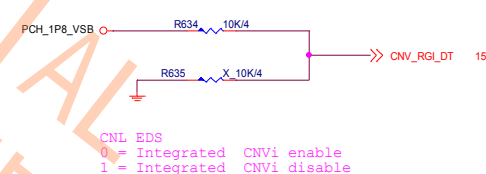


20170814 CHANGE

XTAL FREQUENCY SELECTION

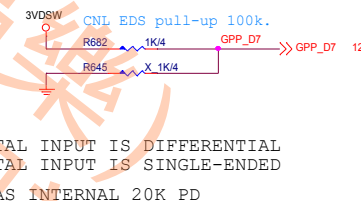


MODEM AND NFC REFERENCE CLOCK SOURCE SELECT



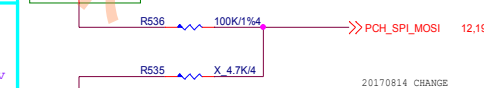
20170816 change

XTAL INPUT MODE



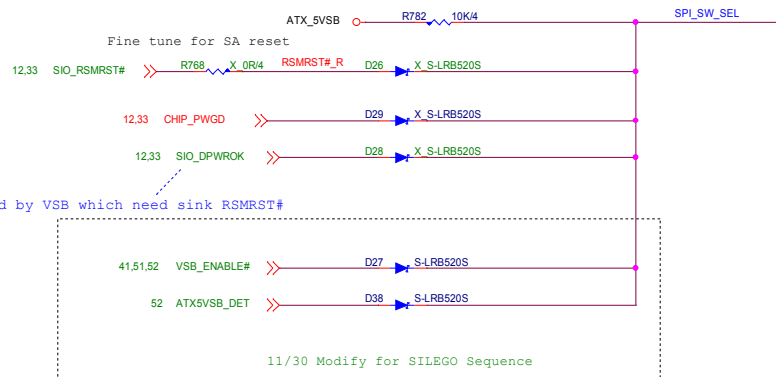
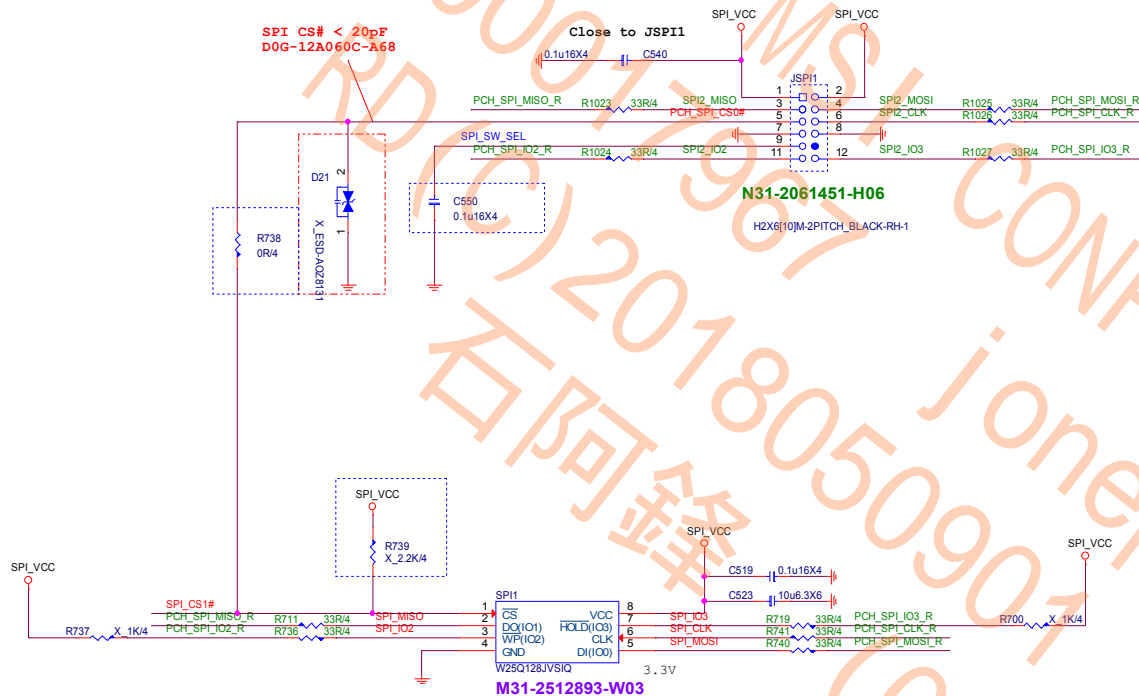
171213 Change to SPI_VCC

Reserved
2017/7/13 from Intel's feedback
R1823 stuff 100Kohm if up to 3.3v
or 75K ohm if up to 1.8v



12	PCH_SPI_CS0#	<<	PCH_SPI_CS0#
12,18	PCH_SPI_MOSI	<<	PCH_SPI_MOSI
12	PCH_SPI_MISO	<<	PCH_SPI_MISO
12	PCH_SPI_CLK	<<	PCH_SPI_CLK
12,18	PCH_SPI_IO2	<<	PCH_SPI_IO2
12,18	PCH_SPI_IO3	<<	PCH_SPI_IO3

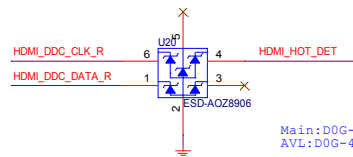
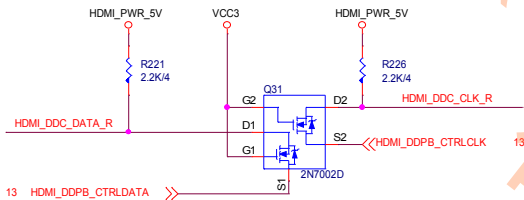
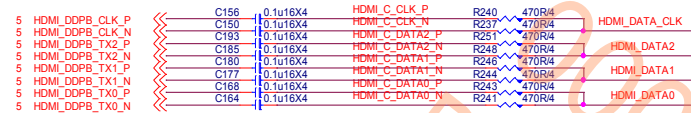
171212 Add for PDG,PDG->5ohm



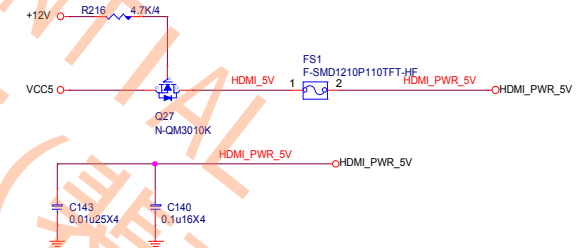
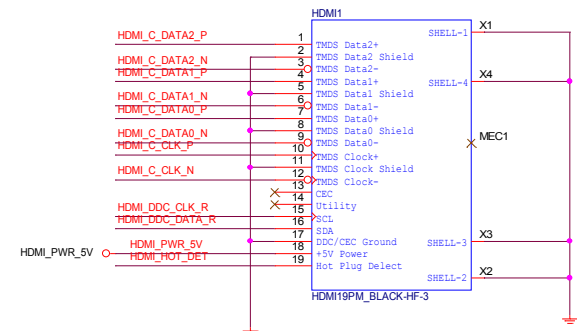
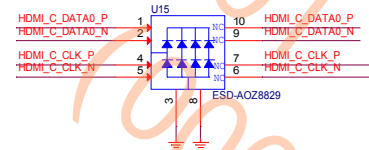
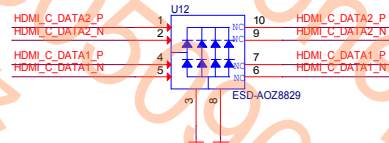
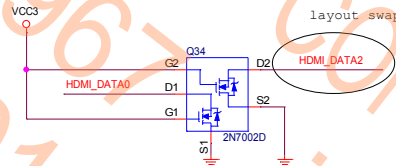
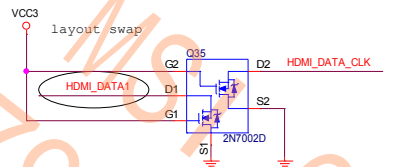
For TL624-1.1 (SKYLAKE)
In skylake, PCH core is powered by VSB which need sink RSMRST#
to low by SPI_SW_SEL.

11/30 Modify for SILEGO Sequence

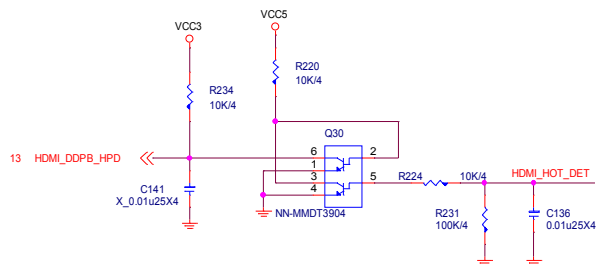
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



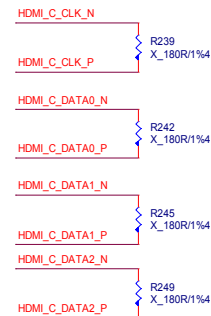
Main:D0G-05A0529-A68
AVL:D0G-45B0510-II14



HPD



For EMI

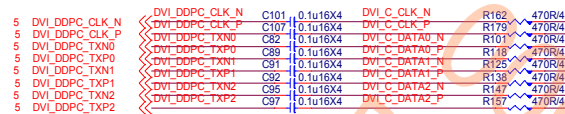


msi

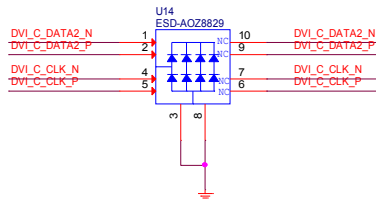
MICRO-STAR INT'L CO.,LTD.

Title			HDMI Connector
Size	Document Number	Rev	
	MS-7B19...	10	
Date:	Tuesday, January 09, 2018	Sheet	20 of 58

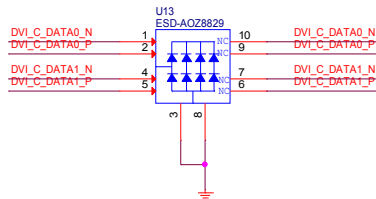
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



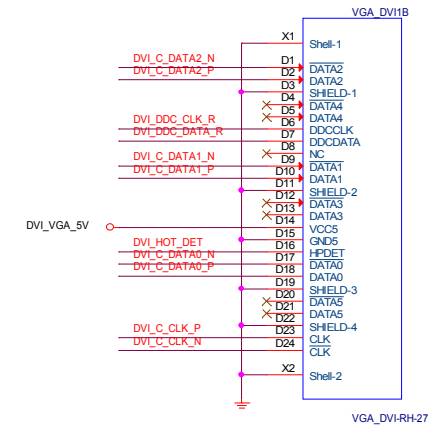
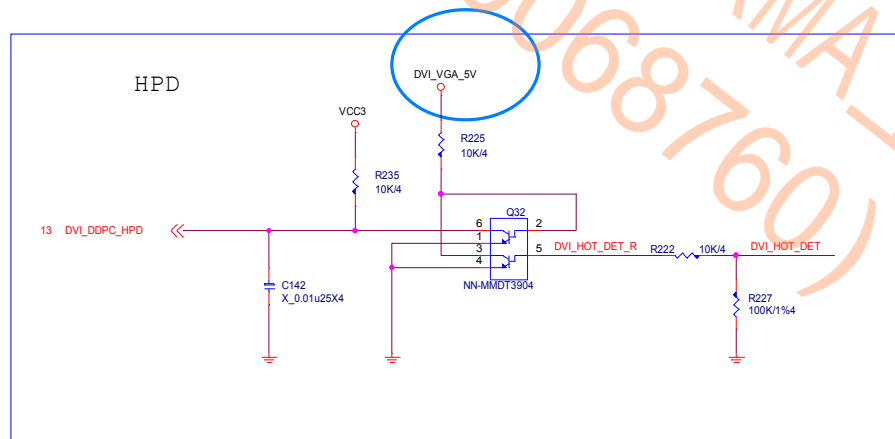
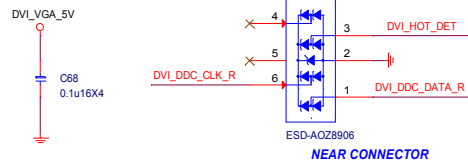
U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



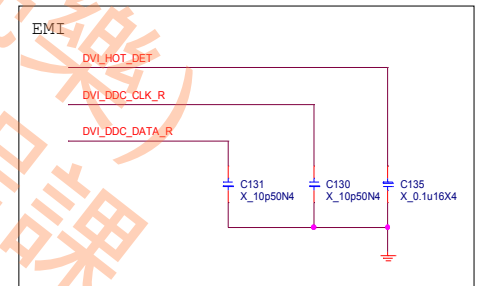
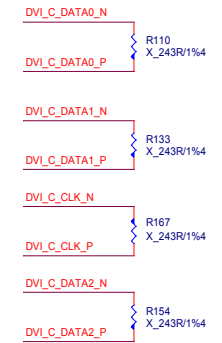
U27 AVL:D0G-05A050C-005
D0G-06A050C-A68



EMI Cap near connector DV11

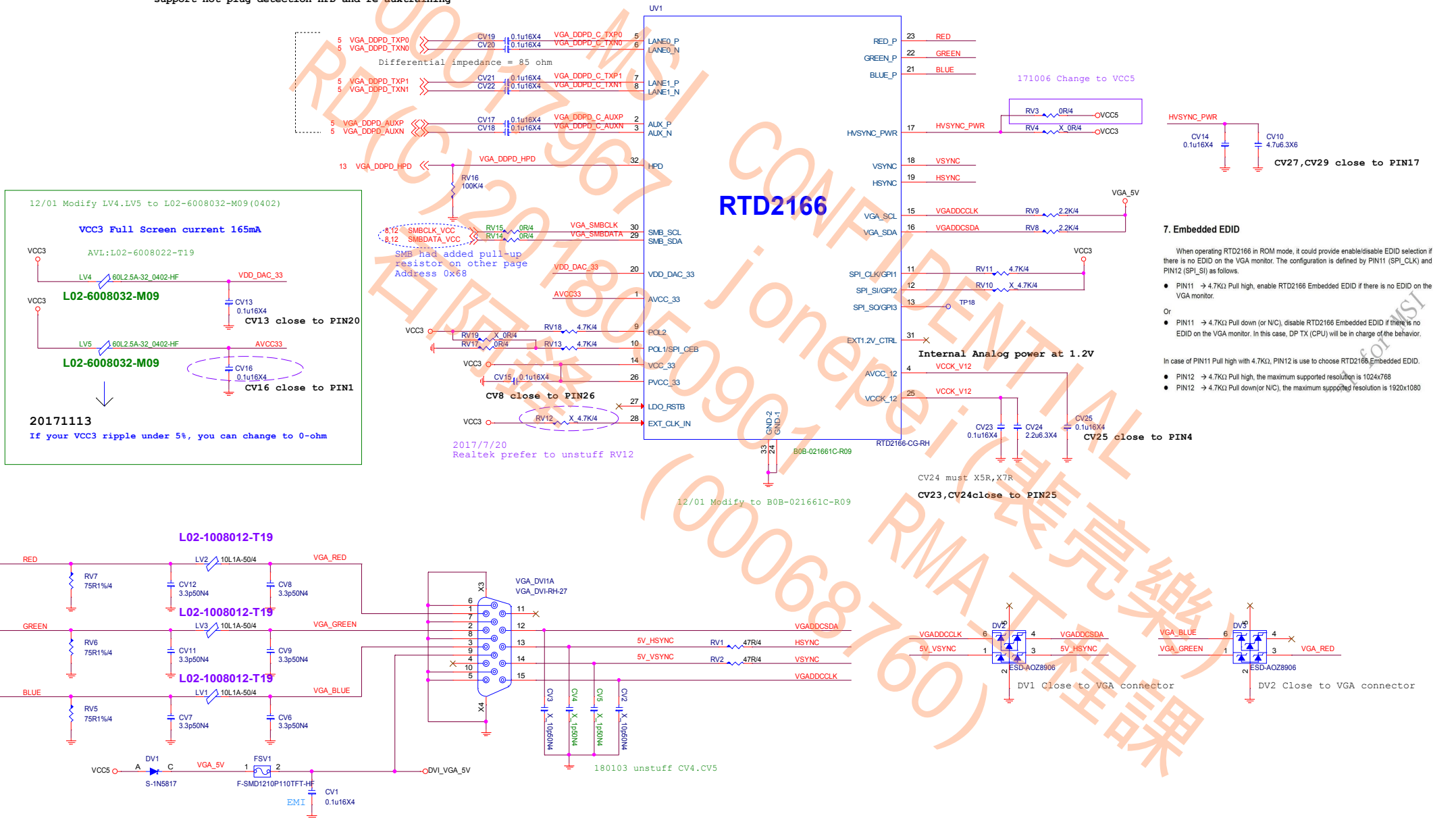


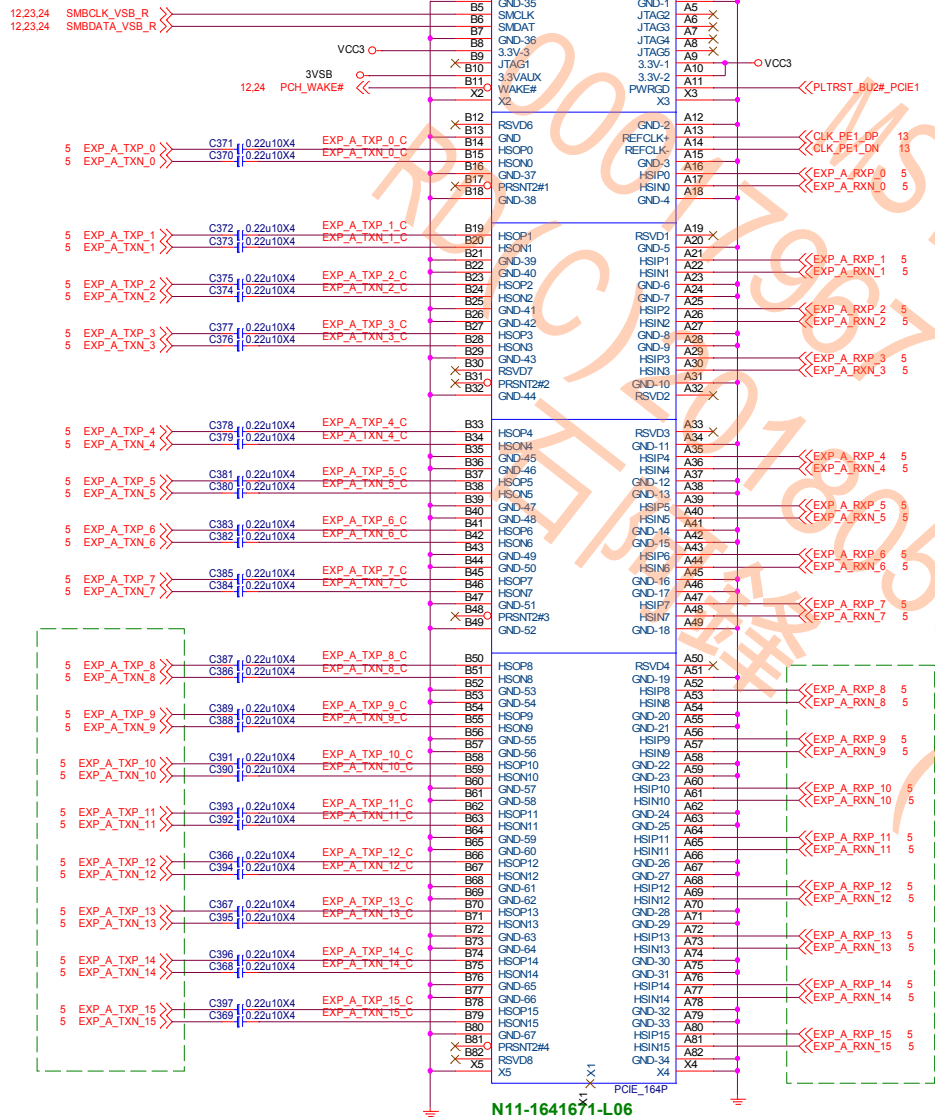
For EMI



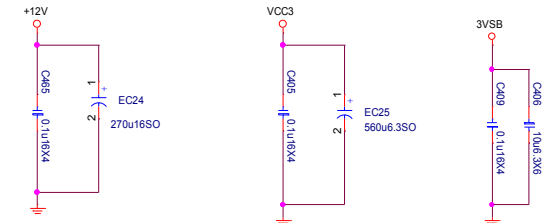
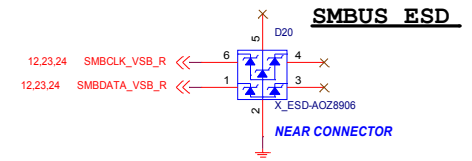
Note:

If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining



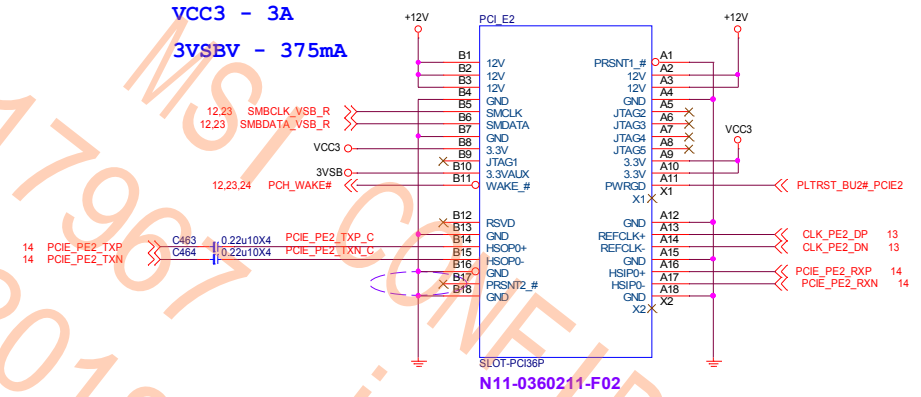


5.5A at +12V
3A at VCC3
375mA at 3VSB

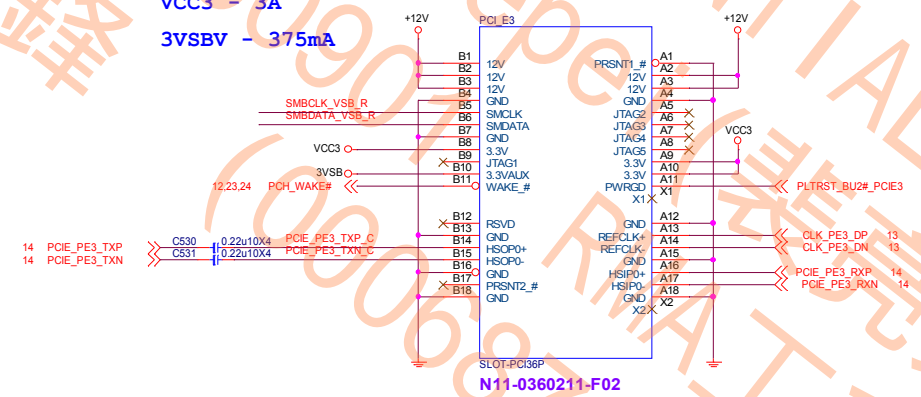


PCH PCIE X1 Slot

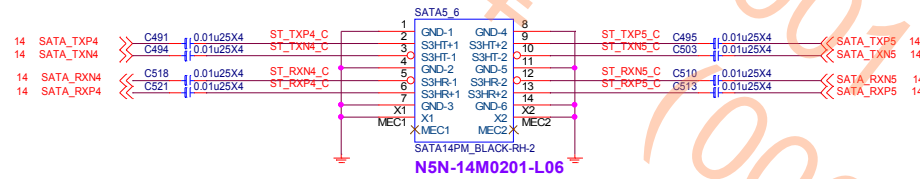
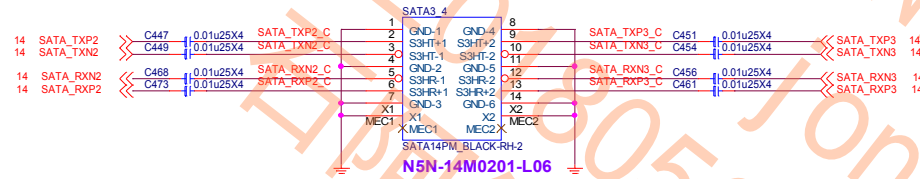
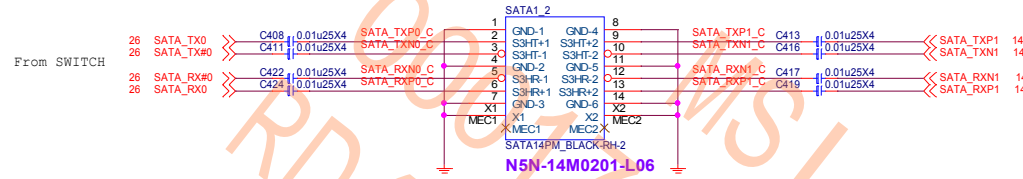
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



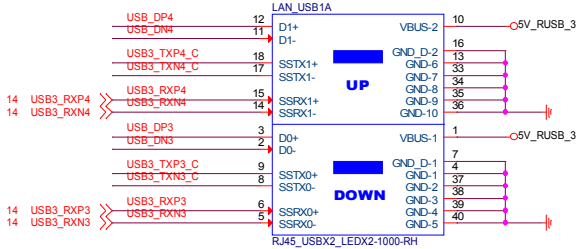
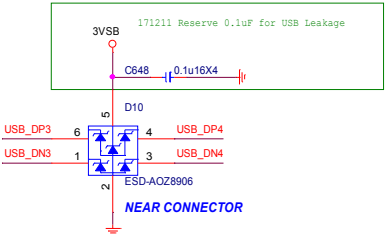
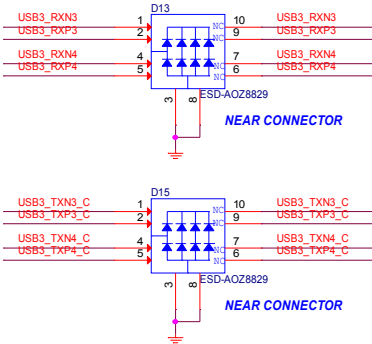
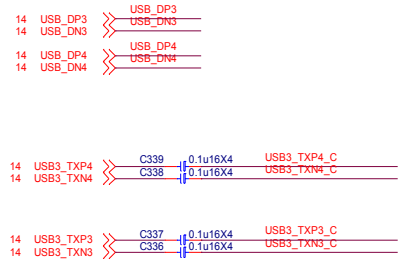
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



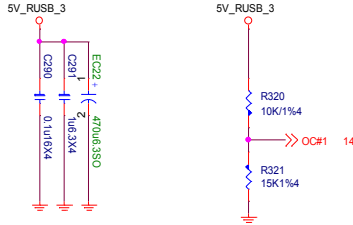
SATA 6G PORT 0.1



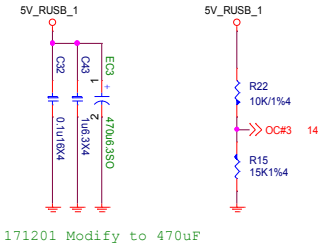
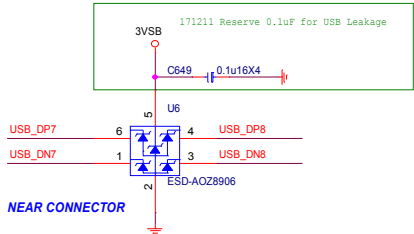
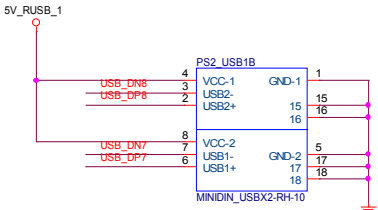
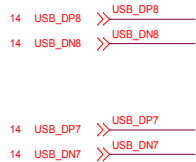
LAN_USB1



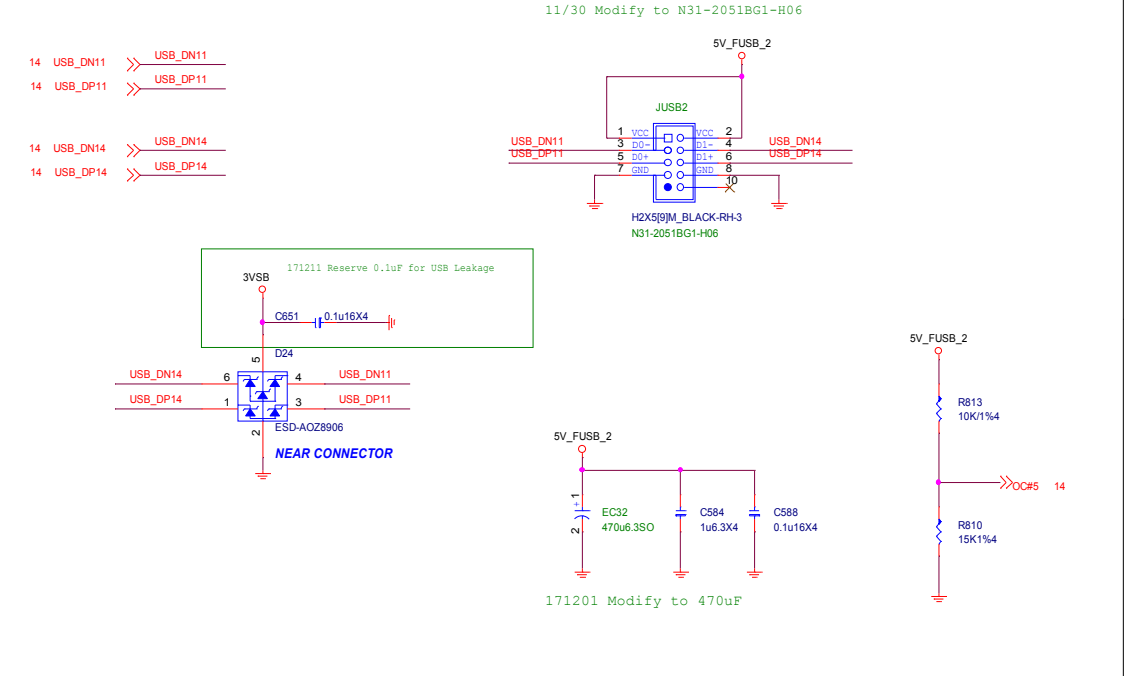
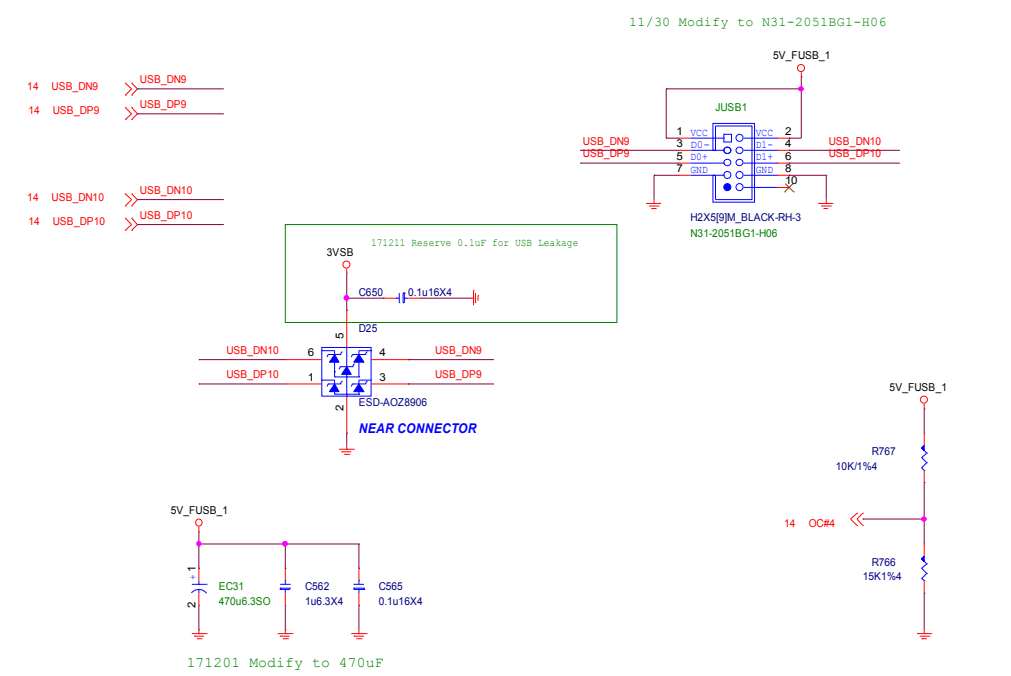
171201 Modify to 470uF



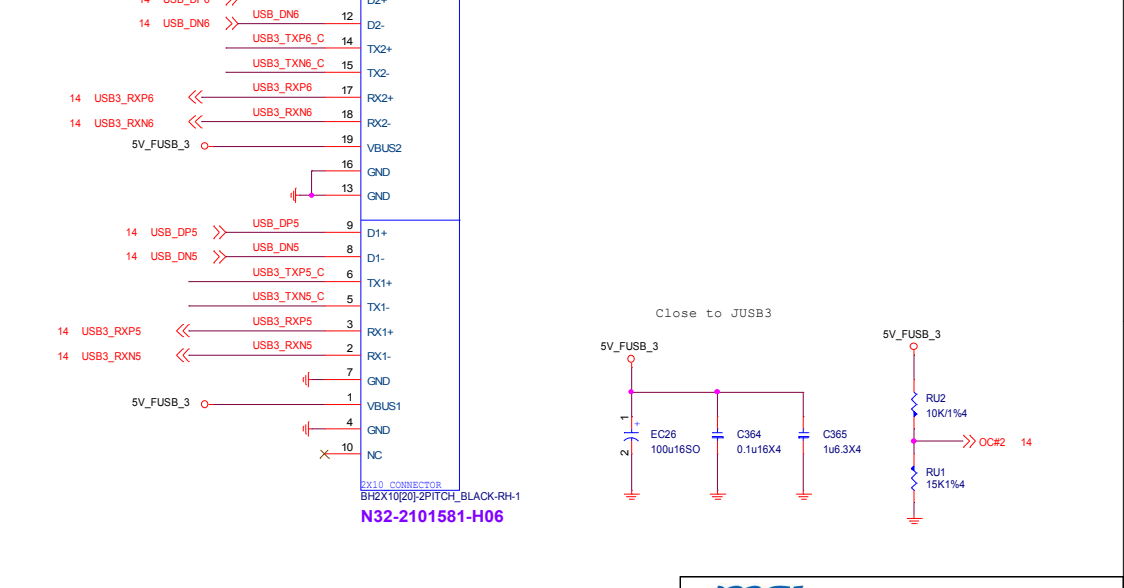
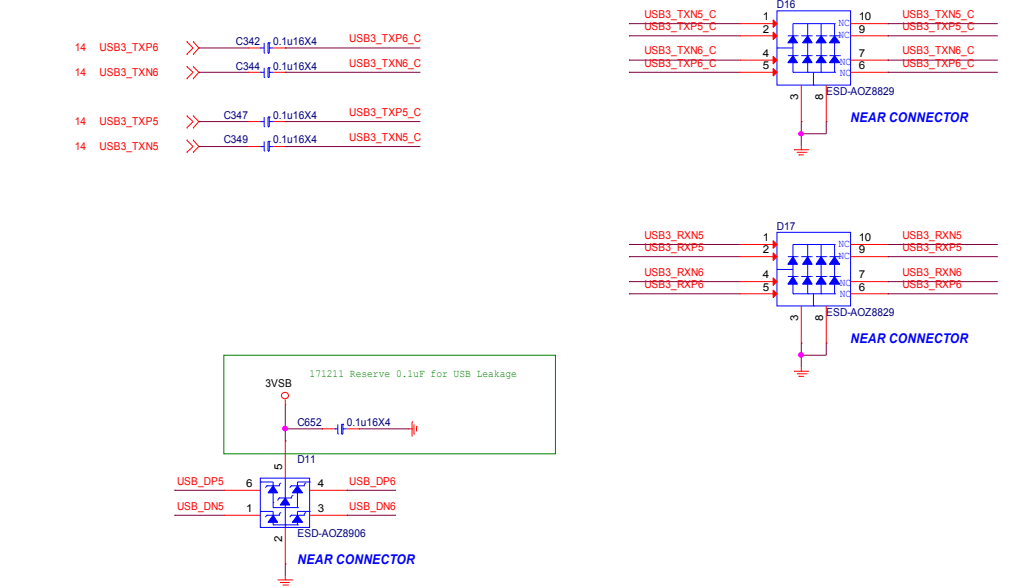
PS2_USB1



FRONT USB2.0



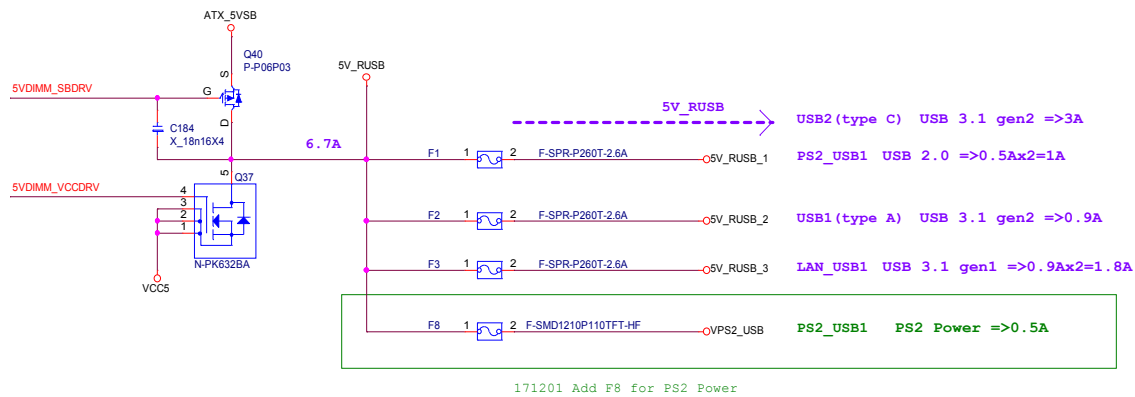
FRONT USB3.0
180



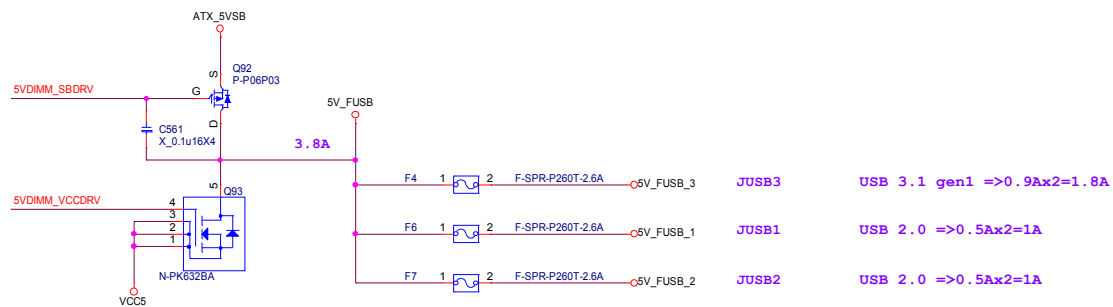
USB POWER



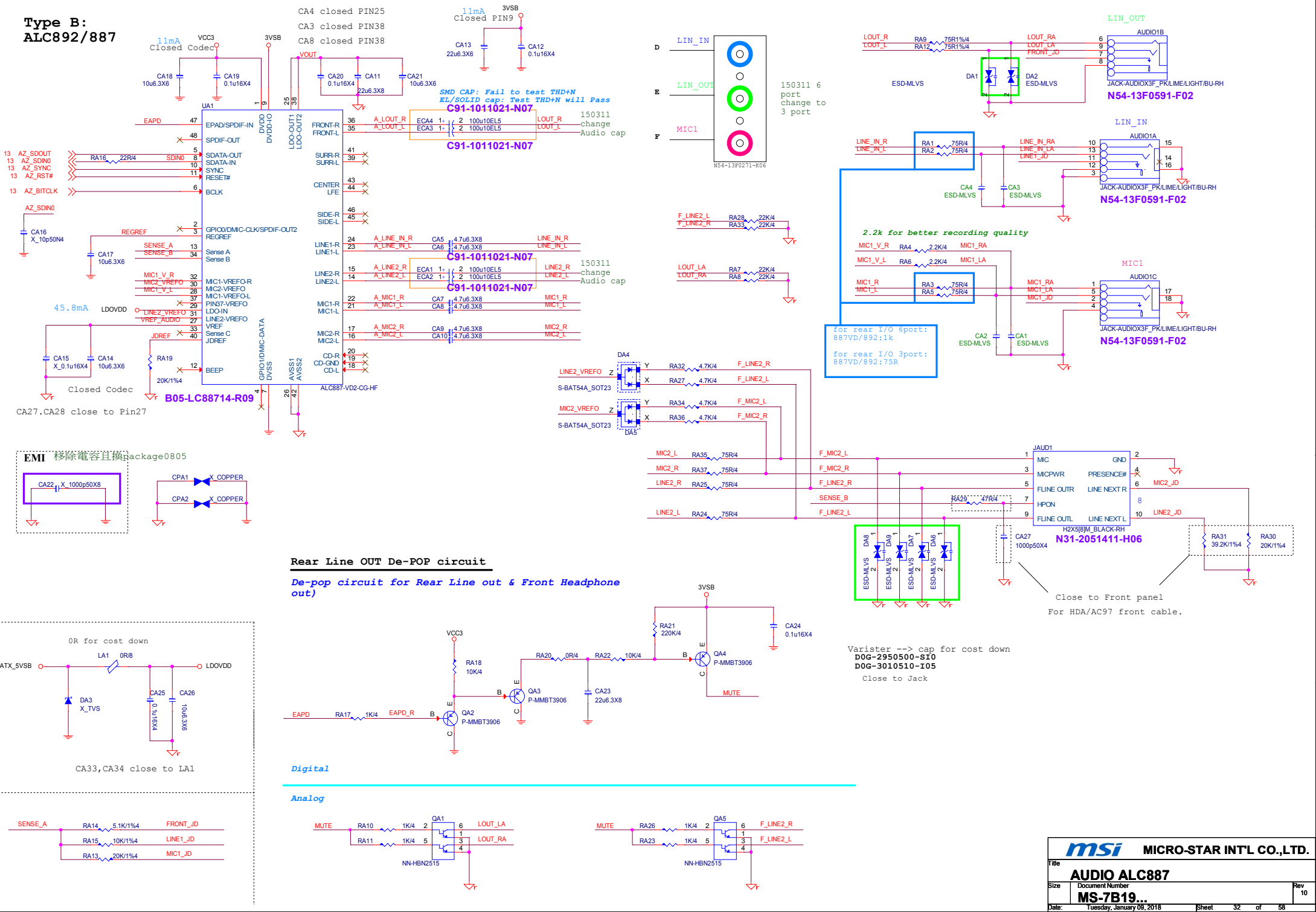
REAR USB PORT POWER



FRONT USB PORT POWER

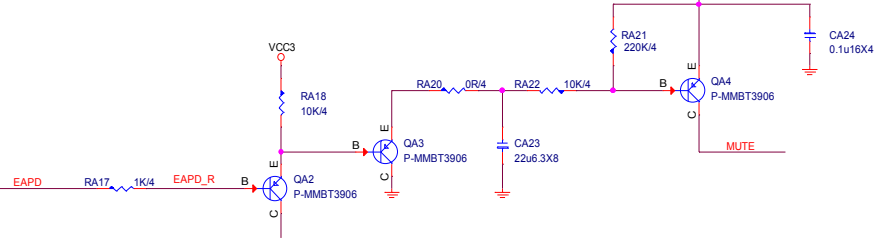


Type B: ALC892/887



Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

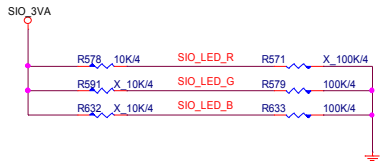


33 PLTRST_BU1# >> R629 100R/1%4 PLTRST_BU1#_LAN 31

33 PLTRST_BU2# >> R651 100R/1%4 PLTRST_BU2#_PCIE1 23
R650 100R/1%4 PLTRST_BU2#_PCIE2 24
R627 100R/1%4 PLTRST_BU2#_PCIE3 24

33 PLTRST_BU3# >> R667 100R/1%4 PLTRST_BU3#_M2_1 26
R672 100R/1%4 PLTRST_BU3#_TPM 53

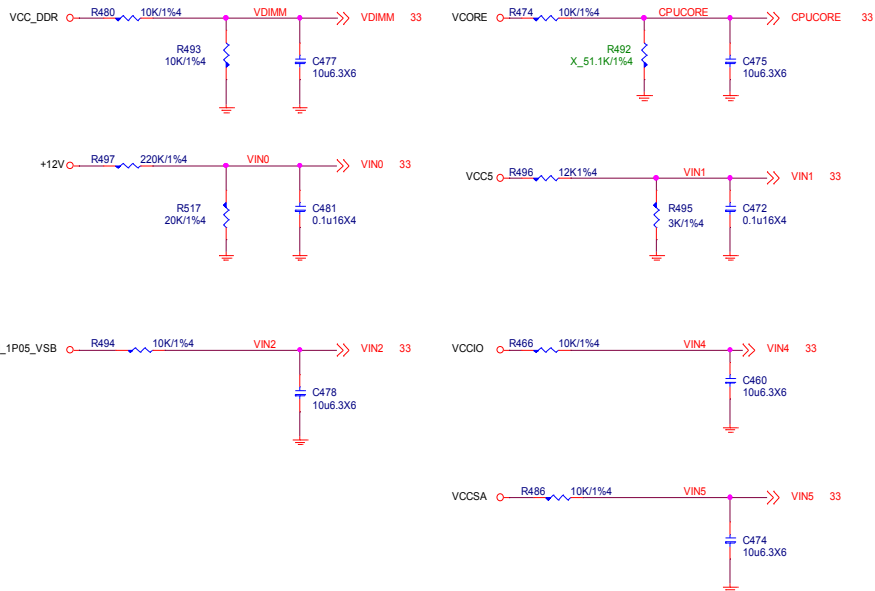
33,38,39 SIO_LED_G >>
33,38,39 SIO_LED_B >>
33,38,39 SIO_LED_R >>



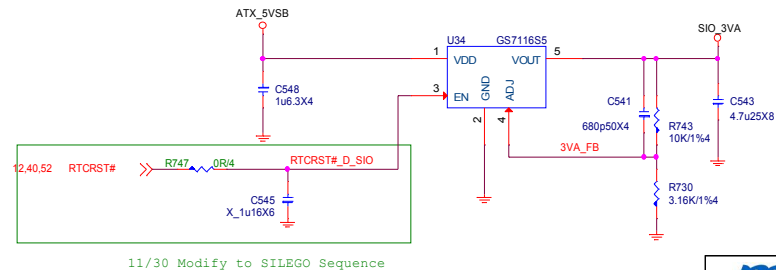
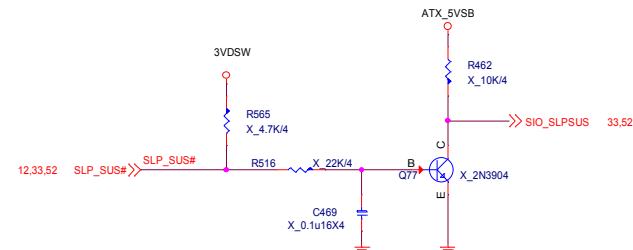
11/30 Remove PCH_1P05_VSB to RSMRST# Circuit

HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect

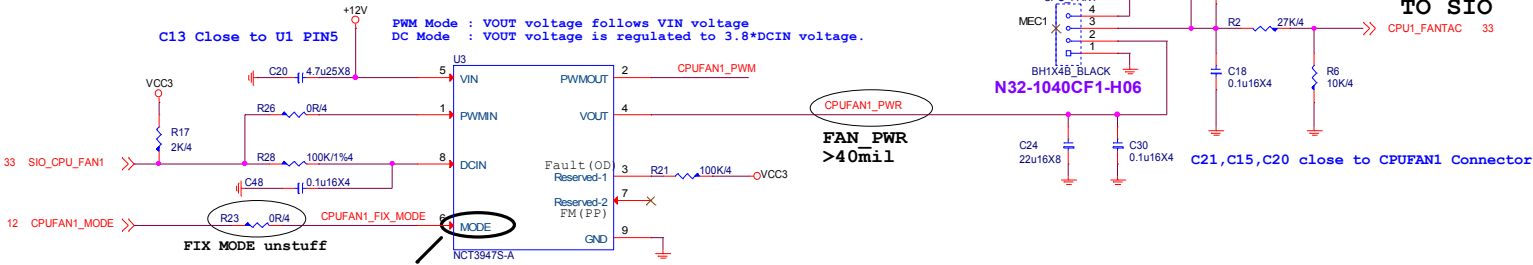


SLP_SUS Co-lay circuit



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
- 2. GPIO可以由BIOS切換 PWM/DC MODE
- 3. OCF拉回GPIO給BIOS認
- 4. PWM OR DC FAN拉回GPIO給BIOS認
- 5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化

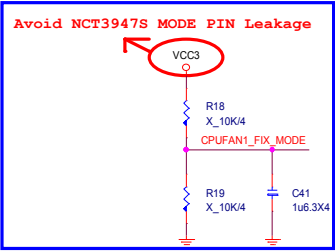


GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default

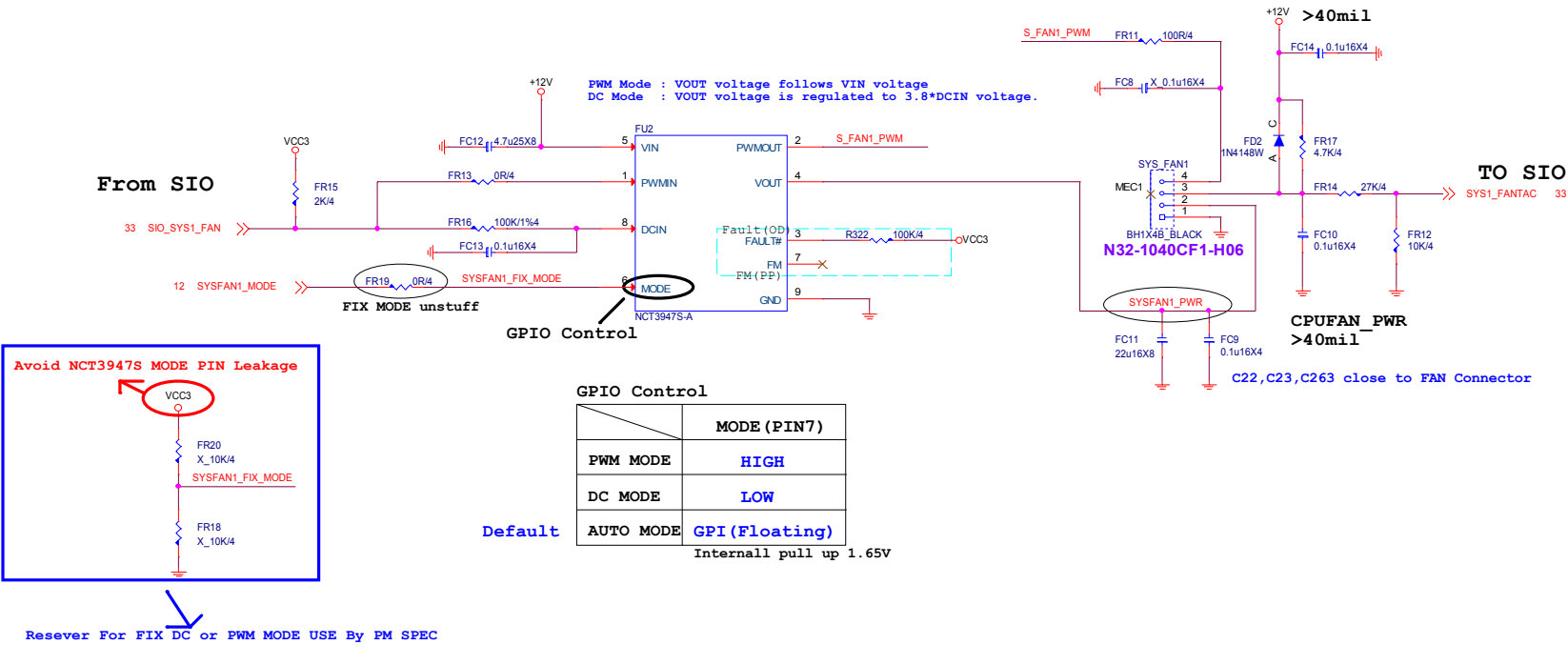
Internall pull up 1.65V



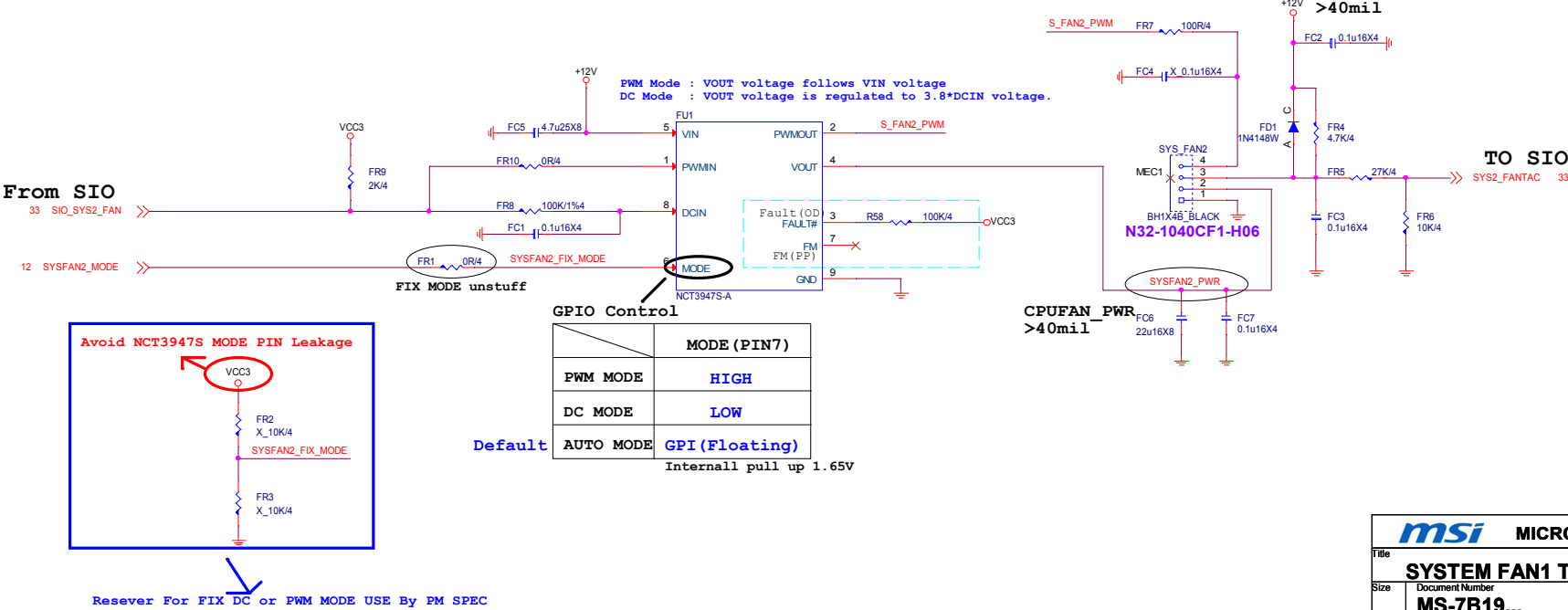
Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE

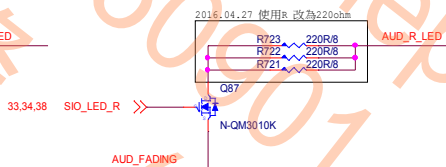
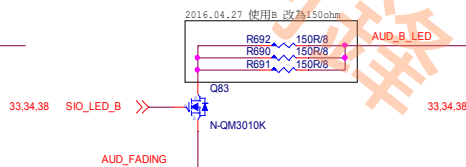
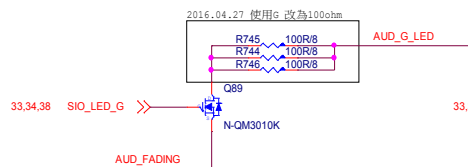
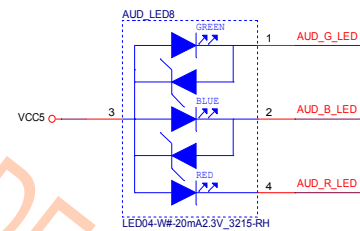
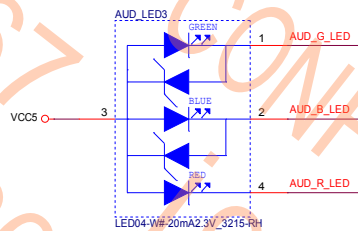
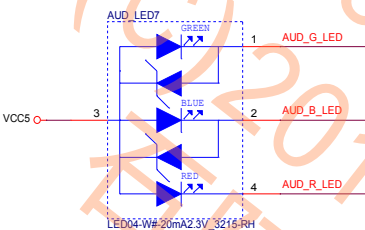
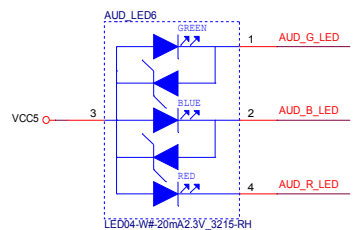
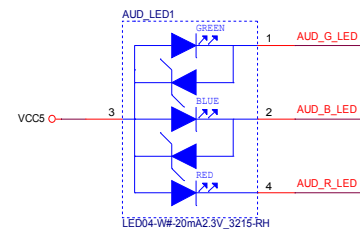
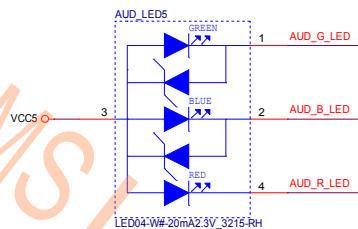
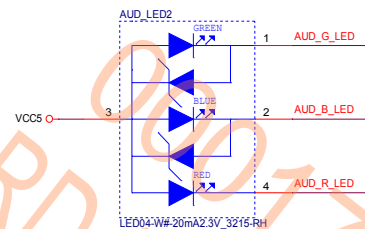
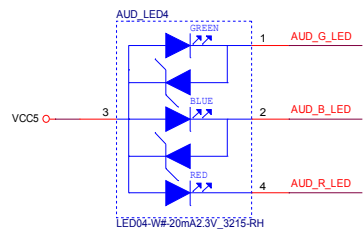


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



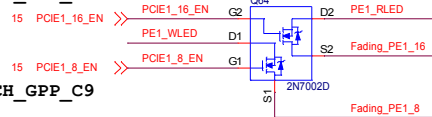
AUDIO_LED

Audio moat is transparent and width 40mil

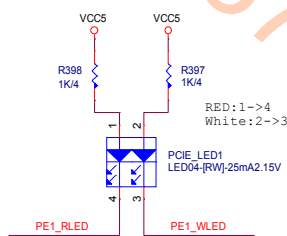
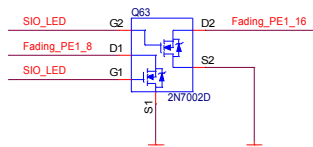


PCIE1_LED

PCH_GPP_C8



PCH_GPP_C9

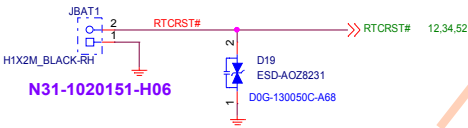


msi

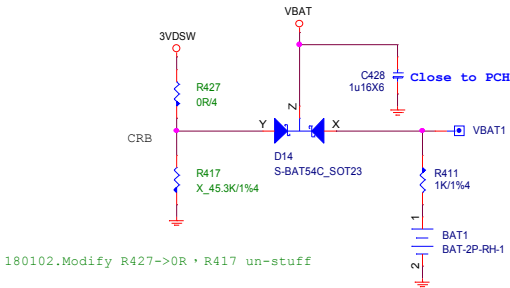
MICRO-STAR INT'L CO.,LTD.

Title	PCIE/AUDIO LED	Rev	10
Size	Document Number		
	MS-7B19...		
Date	Tuesday, January 09, 2018	Sheet	39 of 58

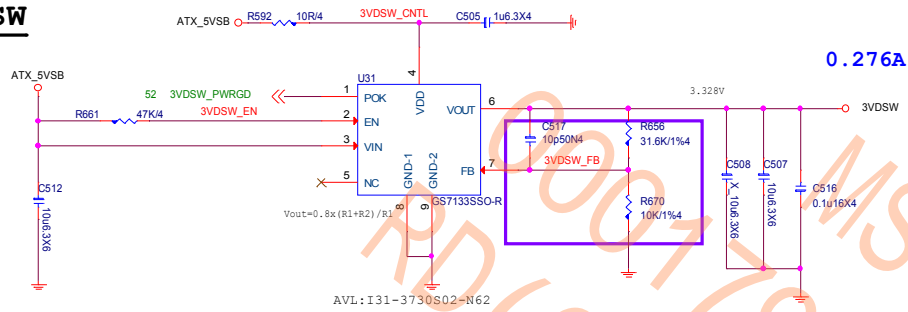
CUT VBAT



VBAT

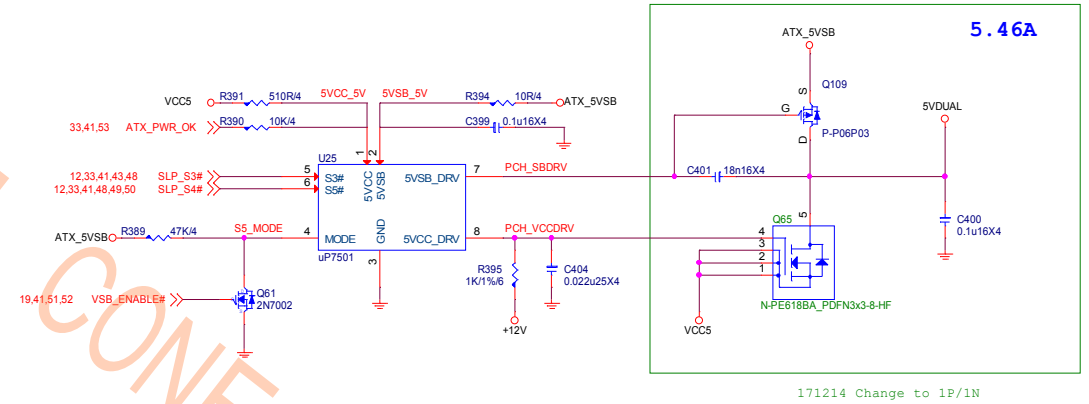


3VDSW

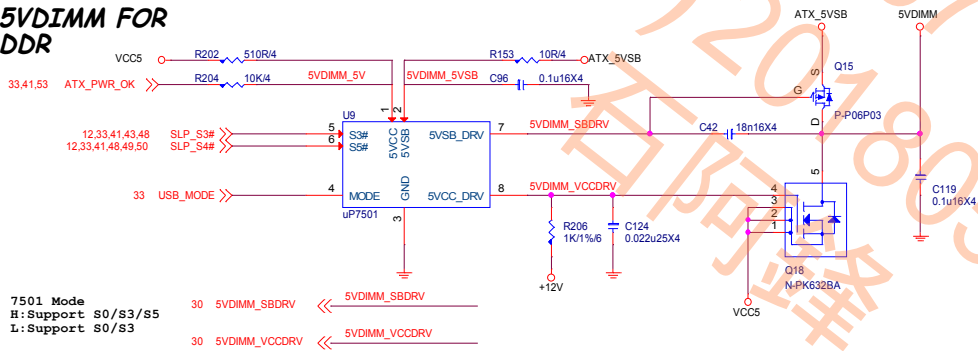


5VDUAL

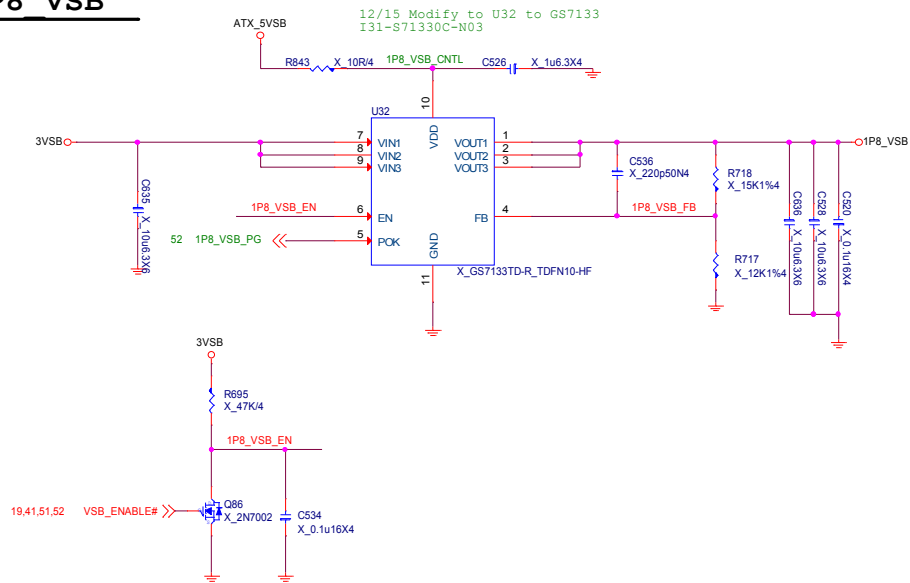
5VDUAL is power source of 1P0SB



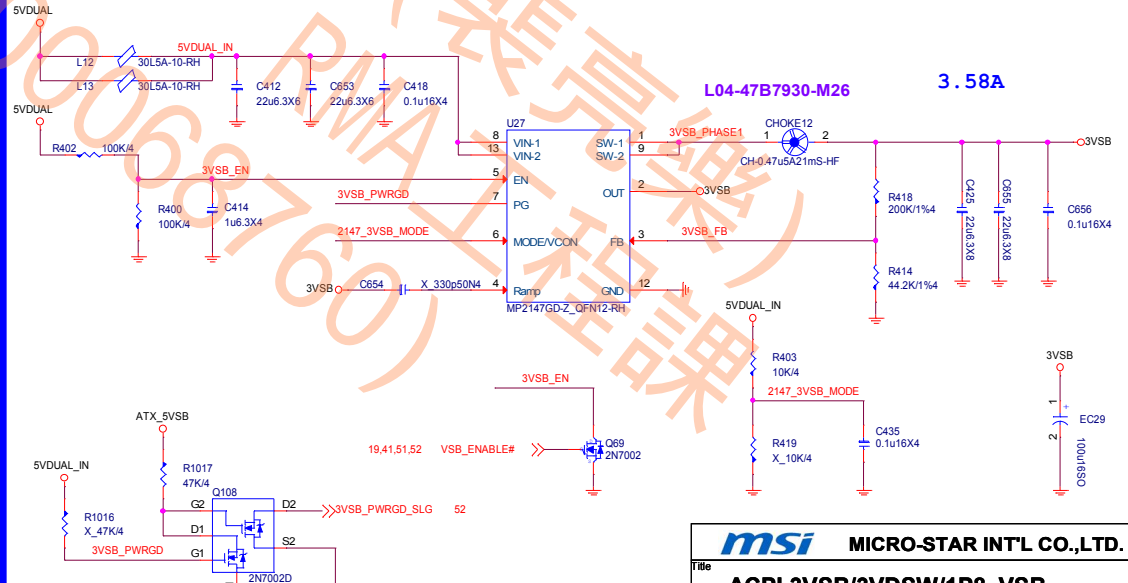
5VDIMM FOR DDR



1P8 VSB

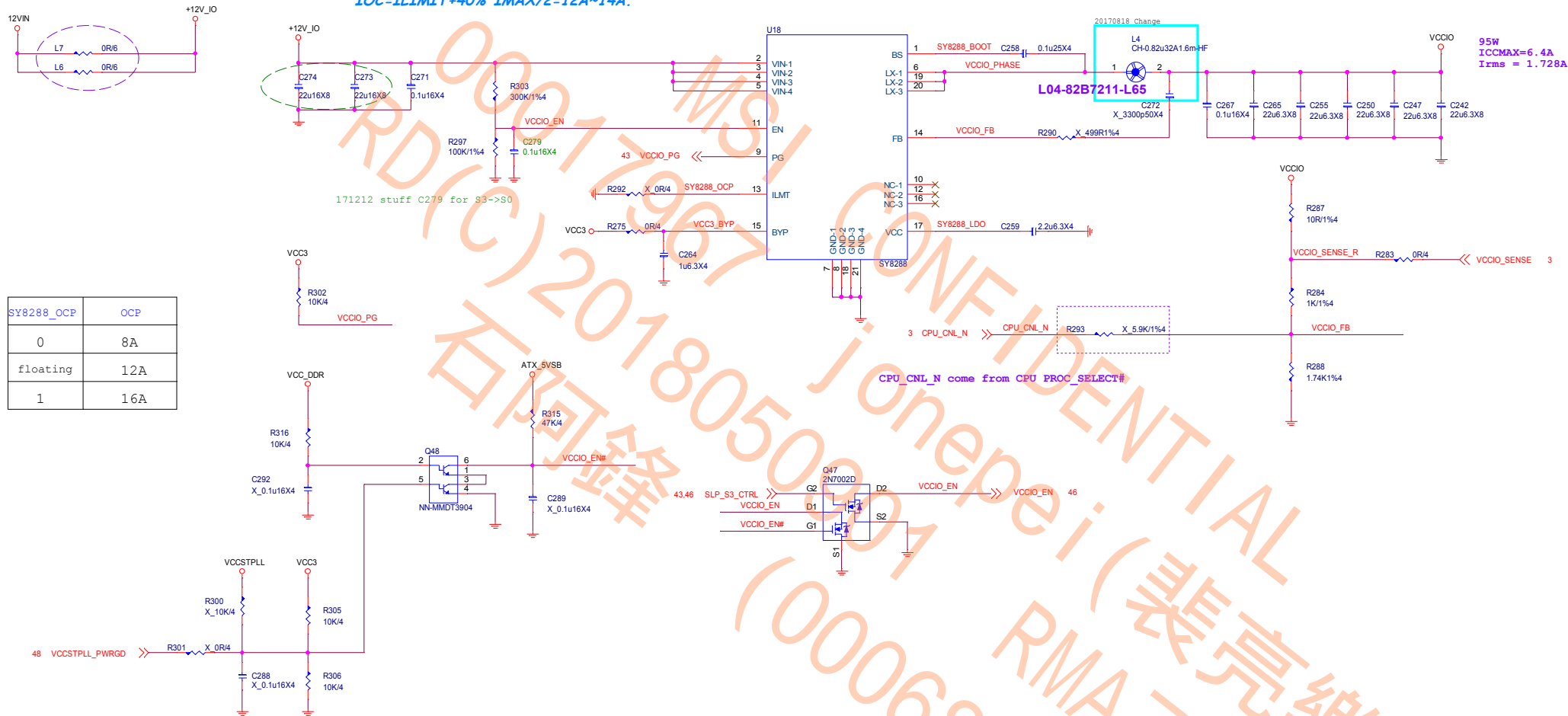


3VSB



IO Power:0.95V,6.4A

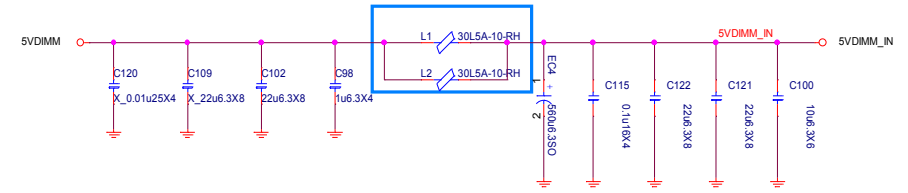
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.



DDR4_1.2V 3.3A+ 7.85A+0.375A=11.525A

3.3A FOR CPU
7.85A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

$I_{in} = 9.525A \times 1.2V / 0.8 / 5V = 2.8575A$
L02-3008043-M26
Over 85°C, Rated Current 1.5A.



VID	Reference Voltage (V)
H	0.675
L	0.75

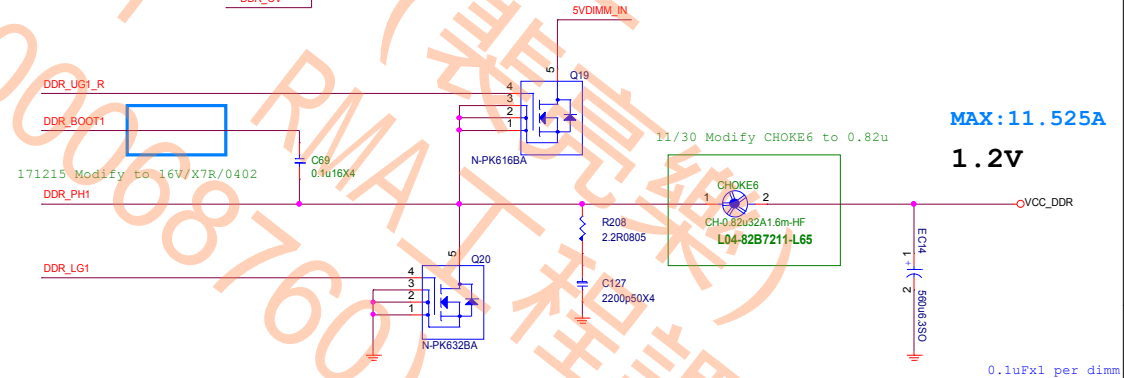
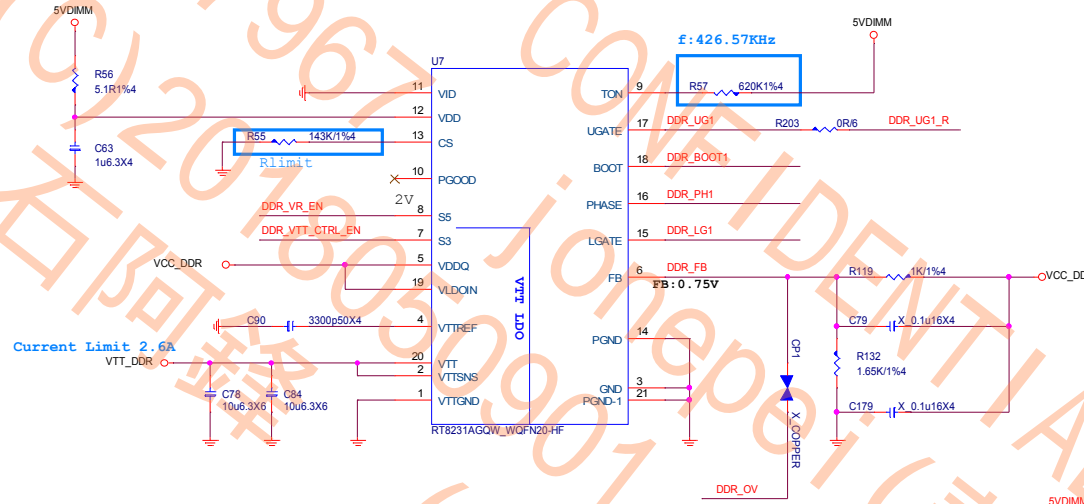
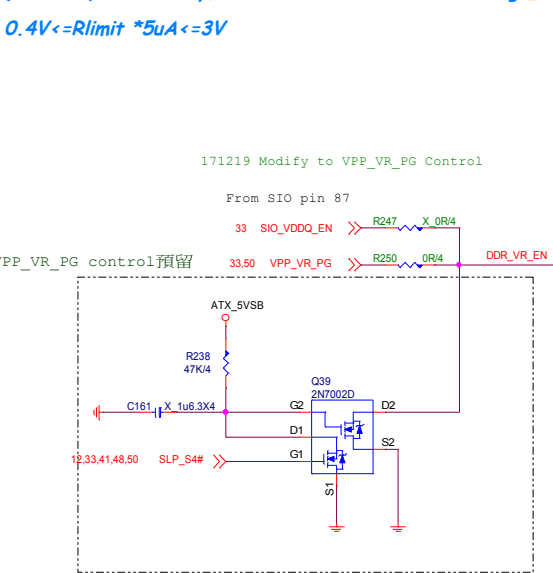
$$I_{rms} = I_{out} \times \sqrt{((V_{out}/V_{in}) \times (1 - (V_{out}/V_{in})))}$$
$$= 9.525 \times 0.427$$
$$= 4.06797A$$

D03-4503NOC-ST8
Current limit= $143K \times 5uA / 10 / 5.1mohm = 14.02A$

D03-632BA0C-N03
Current limit= $143K \times 5uA / 10 / 4.6mohm = 15.54A$

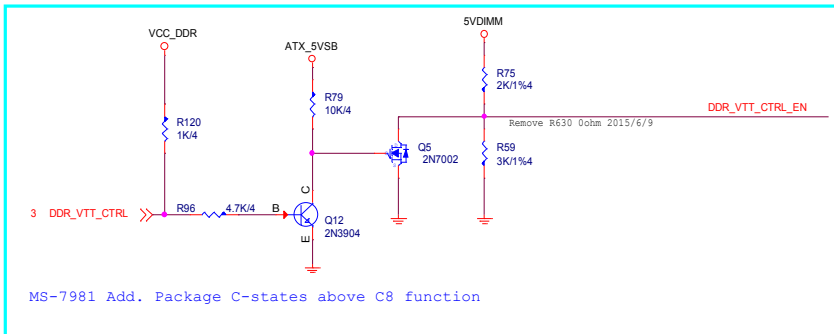
D03-3109M00-U47
Current limit= $143K \times 5uA / 10 / 2.5mohm = 28.6A$
(If UBIQ used finally, Rlimit need to be Calculated again.)

$0.4V \leq R_{limit} \times 5uA \leq 3V$



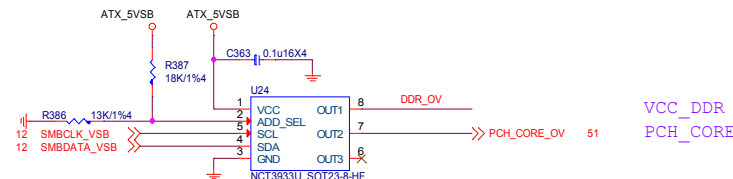
SLP_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down



UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

